What is claimed is:

1. A method of performing a conditional vector output operation in a processor, the method comprising:

receiving electrical signals representative of an input vector;

receiving electrical signals representative of a condition vector, the number of values in the input vector being equal to the number of values in the condition vector, values in the input vector and in the condition vector being in one-to-one correspondence with one another, and each value in the condition vector being a result of evaluating a predetermined conditional expression using data corresponding to a value in the input vector; and

generating electrical signals representative of an output vector containing values in the input vector for which corresponding values in the condition vector are equal to a predetermined value, a length of the output vector being equal to a number of values in the condition vector that are equal to the predetermined value.

2. The method of claim 1, wherein the predetermined conditional expression is a Boolean expression.

3. The method of claim 1, further comprising:

generating electrical signals representative of at least one additional output vector containing values in the input vector for which corresponding values in the condition vector are not equal to the predetermined value, wherein a plurality

of output vectors comprise the output vector and the at least one additional output vector.

4. The method of claim 3, wherein each value in the input vector is in one and only one of the plurality of output vectors.

5. The method of claim 3, wherein generating the plurality of output vectors includes, for each value in the condition vector, including one of the corresponding values in the input vector in one of the plurality of output vectors.

6. The method of claim 3, further comprising:

processing portions of the electrical signals corresponding to each of the plurality of output vectors using the processor, the processing for at least two of the output vectors being different from one another.

7. A method of performing a conditional vector output operation in a processor, the method comprising:

receiving electrical signals representative of an input vector;

receiving electrical signals representative of a condition vector, the number of values in the input vector being equal to the number of values in the condition vector, values in the input vector and in the condition vector being in one-to-one correspondence with one another, and each value in the condition vector being a result of evaluating a predetermined conditional expression using data corresponding to a value in the input vector;

generating electrical signals representative of an output vector containing values in the input vector for which corresponding values in the condition vector are equal to a predetermined value; and

storing successive values of the output vector in successive locations in a memory device so that a number of locations in the memory device occupied by stored values of the output vector is equal to a length of the output vector.

8. A method of performing a conditional vector output operation in a processor, the method comprising:

receiving electrical signals representative of an input vector;

receiving electrical signals representative of a condition vector, the number of values in the input vector being equal to the number of values in the condition vector, values in the input vector and in the condition vector being in one-to-one correspondence with one another, and each value in the condition vector being a result of evaluating a predetermined conditional expression using data corresponding to a value in the input vector;

generating electrical signals representative of an output vector containing values in the input vector for which corresponding values in the condition vector are equal to a predetermined value; and

storing successive values of the output vector in successive locations in a memory device so that a number of locations in the memory device occupied by stored values of the output vector is equal to the number of values in the input

vector for which corresponding values in the condition vector are equal to the predetermined value.

9. A method of performing a conditional vector output operation in a parallel processor having a plurality of clusters therein, the method comprising:

receiving electrical signals representative of an input vector;

receiving electrical signals representative of a condition vector, the number of values in the input vector being equal to the number of values in the condition vector, values in the input vector and in the condition vector being in one-to-one correspondence with one another, and each value in the condition vector being a result of evaluating a predetermined conditional expression using data corresponding to a value in the input vector;

using the clusters to generate electrical signals representative of an output vector containing values in the input vector for which corresponding values in the condition vector are equal to a predetermined value; and

storing a value of the output vector in a cluster different from a cluster which generated that value.

10. A method of performing a distributed conditional vector input operation in a processor, the method comprising:

generating a plurality of electrical signals as a condition vector representative of whether individual arithmetic clusters in a plurality of arithmetic clusters are to receive data;

distributing a plurality of electrical signals as an input vector having input vector elements to arithmetic clusters in the plurality of arithmetic clusters for which a corresponding portion of the condition vector is equal to a predetermined value, a length of the condition vector being greater than a length of the input vector;

using the arithmetic clusters to process the input vector elements distributed thereto; and

assembling the processed input vector elements to form an output vector having a length equal to that of the condition vector.

11. A method according to claim 10 wherein the corresponding portion of the condition vector comprises corresponding condition vector elements, and wherein a certain plurality of arithmetic clusters receive input vector elements as a result of corresponding condition vector elements for the certain plurality of arithmetic clusters being equal to the predetermined value.

12. A method of performing a conditional vector input operation in a processor, the method comprising:

generating a plurality of electrical signals as a condition vector representative of whether individual arithmetic clusters in a plurality of arithmetic clusters are to receive data;

providing a plurality of electrical signals as an input vector having input vector elements to arithmetic clusters in the plurality of arithmetic clusters for which corresponding condition vector elements of the condition vector are equal to

a predetermined value, the number of clusters being greater than the number of input vector elements, the input vector elements being in one-to-one correspondence with corresponding condition vector elements of the condition vector that are equal to the predetermined value;

using the arithmetic clusters to process the input vector elements provided thereto; and

assembling the processed input vector elements to form an output vector.

13. A method of performing a conditional vector input operation in a processor, the method comprising:

generating a plurality of electrical signals as a condition vector representative of whether individual arithmetic clusters in a plurality of arithmetic clusters are to receive data;

providing a plurality of electrical signals as an input vector having input vector elements to arithmetic clusters in the plurality of arithmetic clusters for which corresponding condition vector elements of the condition vector are equal to a predetermined value, the number of clusters being greater than the number of input vector elements, the input vector having only input vector elements corresponding to condition vector elements of the condition vector that are equal to the predetermined value;

using the arithmetic clusters to process the input vector elements provided thereto; and

assembling the processed input vector elements to form an output vector.

14. A method of performing a distributed conditional vector input operation in a processor, the method comprising:

generating a plurality of electrical signals as a condition vector representative of whether individual arithmetic clusters in a plurality of arithmetic clusters are to receive data;

distributing a plurality of electrical signals from a storage area in at least one cluster as an input vector to arithmetic clusters in the plurality of arithmetic clusters for which a corresponding portion of the condition vector is equal to a predetermined value, a length of the condition vector being greater than a length of the input vector;

using the arithmetic clusters to process input vector elements of the input vector distributed thereto;

assembling the processed input vector elements to form an output vector having a length equal to that of the condition vector; and

storing an output vector element of the output vector in a storage area of a cluster different from a cluster from which an input vector element was distributed.

15. A method of performing a conditional vector switching operation in a processor, the method comprising:

receiving electrical signals representative of an input vector, the input vector having input vector elements;

receiving electrical signals representative of a condition vector, the condition vector having condition vector elements, a number of the input vector

elements being equal to a number of the condition vector elements, the input vector elements and the condition vector elements being in one-to-one correspondence with one another, and each condition vector element being a result of evaluating a predetermined conditional expression using data corresponding to an input vector element;

generating electrical signals representative of an intermediate vector, the intermediate vector having intermediate vector elements that contain input vector elements for which corresponding condition vector elements are equal to a predetermined value, a number of intermediate vector elements being equal to a number of condition vector elements in the condition vector that are equal to the predetermined value; and

generating electrical signals representative of an output vector, the output vector having output vector elements in one-to-one correspondence with the intermediate vector elements, each output vector element is a result of a computation performed on each corresponding intermediate vector element.

16. A method of performing a conditional vector switching operation in a processor, the method comprising:

receiving electrical signals representative of an input vector of a first length, the input vector having input vector elements;

receiving electrical signals representative of a condition vector of a second length, the first and second lengths being equivalent, the condition vector having condition vector elements in one-to-one correspondence with the input vector elements, at least one

of the condition vector elements being equal to a value other than a predetermined value, at least one of the condition vector elements being equal to the predetermined value;

generating electrical signals representative of an intermediate vector of a third length, the third length being less than the first length, the intermediate vector having intermediate vector elements in one-to-one correspondence with any condition vector elements being equivalent to the predetermined value, the intermediate vector elements respectively comprising any input vector elements corresponding to any condition vector elements that are equal to the predetermined value; and

performing a computation on each intermediate vector element to generate electrical signals representative of an output vector of a fourth length, the third and fourth lengths being equivalent.

17. A method of performing a conditional vector switching operation in a processor, the method comprising:

receiving electrical signals representative of an input vector, the input vector having input vector elements;

receiving electrical signals representative of a condition vector, the condition vector having condition vector elements, a number of the input vector elements being equal to a number of the condition vector elements, the input vector elements and the condition vector elements being in one-to-one correspondence with one another, and each condition vector element being a result of evaluating a predetermined conditional expression using data corresponding to an input vector element;

generating electrical signals representative of a first intermediate vector, the first intermediate vector having first intermediate vector elements that contain input vector elements for which corresponding condition vector elements are equal to a first predetermined value, a number of first intermediate vector elements being equal to a first number of condition vector elements in the condition vector that are equal to the first predetermined value; and

generating electrical signals representative of a second intermediate vector, the second intermediate vector having second intermediate vector elements that contain input vector elements for which corresponding condition vector elements are equal to a second predetermined value, a number of second intermediate vector elements being equal to a second number of condition vector elements in the condition vector that are equal to the second predetermined value;

generating electrical signals representative of a first output vector, the first output vector having first output vector elements in one-to-one correspondence with the first intermediate vector elements, each first output vector element is a result of a first computation performed on each corresponding first intermediate vector element; and

generating electrical signals representative of a second output vector, the second output vector having second output vector elements in one-to-one correspondence with the second intermediate vector elements, each second

output vector element is a result of a second computation performed on each corresponding second intermediate vector element.

18. A method of performing a conditional vector combining operation in a processor, the method comprising:

receiving electrical signals representative of a first input vector, the first input vector having first input vector elements;

receiving electrical signals representative of a second input vector, the second input vector having second input vector elements;

receiving electrical signals representative of a condition vector, the condition vector having condition vector elements, each condition vector element taking on one of a first condition value and a second condition value; and

generating electrical signals representative of an output vector by examining successive values of the condition vector elements and interleaving first input vector elements for which condition vector elements in the condition vector are equal to the first condition value with second input vector elements for which condition vector elements are equal to the second condition value, a length of the output vector being equal to a length of the condition vector.

19. A method of performing a distributed conditional vector combining operation in a processor, the method comprising:

generating a plurality of electrical signals as a condition vector, the condition vector having condition vector elements, each condition vector element taking on one of a first condition value and a second condition value, the first

and second condition values representative of whether individual arithmetic clusters in a plurality of arithmetic clusters are to receive data from a first input vector or a second input vector;

distributing a plurality of electrical signals as the first input vector, the first input vector having first input vector elements, to arithmetic clusters in the plurality of arithmetic clusters for which the condition vector elements are equal to the first condition value, a length of the condition vector being greater than a length of the first input vector;

distributing a plurality of electrical signals as the second input vector, the second input vector having second input vector elements, to arithmetic clusters in the plurality of arithmetic clusters for which the condition vector elements are equal to the second condition value, the length of the condition vector being greater than a length of the second input vector;

using the arithmetic clusters to process the first input vector elements and the second input vector elements distributed thereto; and

assembling the processed input vector elements to form an output vector having a length equal to the length of the condition vector.

20. A method of performing a distributed conditional vector load balancing operation in a processor, the method comprising:

distributing a plurality of electrical signals as an input vector, the input vector having input vector elements, to successive arithmetic clusters in a plurality of arithmetic clusters;

using the arithmetic clusters to process the input vector elements distributed thereto, each arithmetic cluster completing processing of one input vector element before another input vector element is distributed to the arithmetic cluster, the processing time of any input vector element being dependent on a value of the input vector element; and

assembling the processed input vector elements to form output vector elements of an output vector, each processed input vector element forming at least one output vector element.

21. A method of performing a distributed conditional vector load balancing operation in a processor, the method comprising:

distributing a plurality of electrical signals as an input vector, the input vector having input vector elements, to successive processing elements in a plurality of processing elements; and

generating a plurality of electrical signals representative of an output vector, the output vector having output vector elements; and

for any input vector element,

requesting the input vector element from the input vector;

reading the input vector element into one processing element of the plurality of processing elements;

processing the input vector element for at least one iteration;

generating at least one output vector element from the processed input vector element;

reading an immediately succeeding input vector element, if available, of the input vector elements into any successive processing element of the plurality of processing elements that has completed processing any input vector element;

requesting a successive input vector element, if available, of the input vector elements; and

reading the successive input vector element into the one processing element when the input vector element has been processed.

22. A processor comprising:

a first memory area to store input vector elements;

a second memory area to store condition vector elements, the second memory area having a same length as the first memory area;

a third memory area to store output vector elements, the third memory area having a length equal to a number of condition vector elements that are equal to a predetermined value; and

a logic circuit that transfers input vector elements from the first memory area to the third memory area when corresponding condition vector elements stored in the second memory area are equal to the predetermined value.

23. A processor comprising:

a first memory area to store input vector elements;

a second memory area to store condition vector elements, the second memory area having a same length as the first memory area;

a third memory area to store output vector elements, the third memory area having a length equal to a number of condition vector elements that are equal to a predetermined value; and

a logic circuit that transfers input vector elements from the first memory area to the third memory area when corresponding condition vector elements stored in the second memory area are equal to the predetermined value so that a number of locations in the third memory area occupied by the output vector elements stored in the third memory area is equal to a number of input vector elements for which corresponding condition vector elements are equal to the predetermined value.

24. A processor comprising:

a first memory area to store input vector elements;

a second memory area to store condition vector elements, the second memory area having a same length as the first memory area;

a third memory area to store output vector elements, the third memory area comprising memory locations from plural clusters, the plural clusters generating the output vector elements, the third memory area having a length equal to a number of condition vector elements that are equal to a predetermined value; and

a logic circuit that transfers input vector elements from the first memory area to the third memory area when corresponding condition vector elements stored in the second memory area are equal to the predetermined value to generate

the output vector elements in the plural clusters, wherein an output vector element is stored in a memory location of a different cluster of the plural clusters than that cluster which generated the output vector element.

25. A processor comprising:

a first memory area to store input vector elements;

a second memory area to store condition vector elements, the first memory area having a length equal to a number of condition vector elements that are equal to a predetermined value; and;

a third memory area to store output vector elements, the third memory area having a same length as the second memory area; and

a logic circuit that transfers input vector elements from the first memory area to the third memory area when corresponding condition vector elements stored in the second memory area are equal to the predetermined value.

26. A processor to perform conditional vector operations, including a conditional vector input operation and a conditional vector output operation, comprising:

a first memory area to store an input vector stream, the input vector stream having input vector elements;

a second memory area to store an output vector stream, the output vector stream having output vector elements;

a third memory area to store a condition vector stream, the condition vector stream having condition vector elements;

a buffer having a first plurality of entries and a second plurality of entries to store the input vector elements and the output vector elements;

a plurality of processing elements to process input vector elements into output vector elements;

a switch configured to transfer the input vector elements from the buffer to the processing elements and to transfer the output vector elements to the buffer, the buffer receiving the input vector elements from the first memory area, the buffer receiving the output vector elements from the plurality of processing elements via the switch, the second memory area reading the output vector elements from the buffer, and the plurality of processing elements reading the input vector elements from the buffer via the switch in accordance with the condition vector elements; and

a controller to direct conditional vector input and output operations by controlling reading the input and the output vector elements from the buffer, by controlling receiving the input and the output vector elements into the buffer; by processing the condition vector elements, and by configuring the switch so that the switch is capable of transferring the input and output vector elements between any of the first plurality of entries of the buffer, any of the second plurality of entries of the buffer, and any of the plurality of processing elements.